EXHIBIT F

Paper No. __

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

GOOGLE LLC,
Petitioner,

v.

SINGULAR COMPUTING LLC,
Patent Owner.

Case No. IPR2021-00179
Patent No. 8,407,273

PETITION FOR INTER PARTES REVIEW
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1 et seq.

the examiner) is prior art under pre-AIA § 102(b) even assuming the challenged claims were entitled to their earliest claimed priority date (they are not as Petitioner's concurrently filed petition demonstrates).

Ground Number and Reference(s)		Claims
1	Dockser (Ex. 1007)	1-2, 21-24, 26, 28
2	Dockser, Tong (Ex. 1008)	1-2, 21-24, 26, 28, 32-33
3	Dockser, MacMillan (Ex. 1009)	1-26, 28, 36-61, 63
4	Dockser, Tong, MacMillan	1-26, 28, 32-61, 63, 67-70

Ground 1: Dockser discloses a "floating-point processor" (FPP) that performs "multiplication" at a selectable "precision." Dockser, Abstract, [0012]. Dockser's FPP is an HDR execution unit whose standard floating-point inputs exceed the claimed minimum dynamic range, and which operates at a selectable reduced precision to conserve power in applications where greater precision is unnecessary. A selected "subprecision" is achieved by removing power to any desired number of least-significant mantissa bits, dropping those bits (resulting in less precision) and reducing power consumption. Dockser, [0014]; Goodin, ¶ 388-389. Dockser discloses an example that drops all but the 9 most-significant bits, resulting in imprecision meeting the claimed minimum error amounts. *Infra* § V.B.4.c. Dockser renders obvious claims 1-2, 21-24, 26, and 28.

Dated: November 6, 2020

Respectfully submitted,
Google LLC

By /Elisabeth Hunt/
Elisabeth H. Hunt, Reg. No. 67,336
WOLF GREENFIELD & SACKS, P.C.